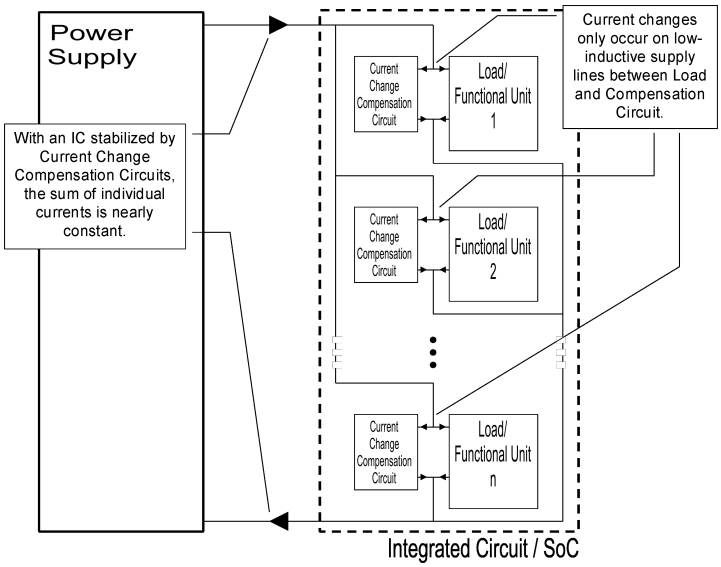
Power Concept for High Frequency Operated Microelectronics

TOPIC

Modern microelectronics causes massive load changes – an IC (Integrated Circuit) or a SoC (System on a Chip) can be seen as a huge number of single loads with switching elements within. While the switching of on and off is close to balance, the power supply lying outside of the IC is able to handle the changes in power consumption reliably. However, this is increasingly complicated with a rising clock frequency, because the voltage stabilization provided by capacitors loses efficiency at 1 GHz and above.
Without the support of capacitors, as early as from 100 MHz on small inductances may lead to a computer crash caused by the voltage drop of a single gate switching from low to high.



The patent application PCT/DE2005/001831 (US 8,466,663) describes a method to avoid these voltage failures. This happens by relieving the discrete power supply. To critical loads within the IC, a current-carrying component is connected in parallel. This component will supply its current to the load when required. As a result, the power consumption of this combination remains nearly constant, reducing requirements to be met by the IC's power supply. The usually effective inductances of supply lines become inoperative; voltage drop or magnification by switching loads is prevented.

This proceeding substitutes or supports capacitors limited in their applicability. Indeed, the consumption of the IC rises by the current carried in parallel. At the same time, measures to dejam signals or to diminish interferences that have been necessary up to now will become obsolete. Therefore, in sum the current demands of the overall system decrease.

SUCCESSIONS

- Clock Rates beyond 10 GHz become possible
- Reduced Power Consumption
- Increased Reliability
- Suppression of Electrical Noise
- Established Structure Sizes can be maintained
- Simplified Integrated Circuit Design
- Less Wafer Space and Layers are required
- Faster Production
- Production on Lines in Use

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Additional notes:

I. Preferred field of application of the patent: Prevention of functional impairing transient noise within high frequency operated integrated circuits

Most of the analogous electronic circuits and data processing digital electronic circuits are in need of a constant operating voltage in order to fulfill their purpose faultlessly. Those circuits therefore need current supply circuits that are capable of using a current supply source of insufficient constancy for providing the circuits' desired operating voltages within their particular stability tolerance.
An operating voltage which is still constant at the current supply circuit gets fed via current supply lines to the electronic circuits needing provision. Dynamic operating current changes of the electronic circuits induce voltage transients at the inductances of the supply lines which get superimposed on the operating voltages of the electronic circuits. If the operating voltage's immunity tolerance of an electronic circuit gets exceeded this may lead to malfunction or even a total breakdown of the electronic circuit despite constant current supply voltages from the operating voltage supply.

The patent describes a universally applicable, fundamental principal to avoid malfunctions of electronic circuits, which is adaptable for any operating frequency:

The arrangement of a dynamic current change compensation circuit in immediate vicinity of the current change source as shunt control connected in parallel to the operating voltage within the electronic circuit. This arrangement prevents operating voltage transients which, when doing without this current change compensation circuit, would otherwise have been induced at the current supply lines due to dynamic current changes of the electronic circuit and which could lead to malfunction of the electronic circuit.

The immediate vicinity is a relative size which is dependent on the dimensions of the current change source and which in principal means "as close as possible". The geometric distance between the current change compensation circuit and the current change source is smaller than their sizes and proportional to their geometric sizes.

From the physics of classical electrodynamics it is known that the inductance of a conductor is proportional to its length and that the voltage induced at an inductance is proportional to the current change rate of the current flowing through this conductor. The current change rate is therefore also proportional to the current change frequency and in turn the current change frequency is (indirectly) proportional to the operating frequency, respectively the clock frequency, of the electronic circuit.

At a given transient tolerance of for example +/- 5% of the operating voltage U_{Op} (depending on the purpose and the architectural implementation of the electronic circuit) and with the electronic's maximally generated current change rate dI/dt, the conductor's maximal inductance L, respectively the conductor's length, for a still error-free operation of the electronic circuit can be derived via the law of inductance. $L = U_{Op} \cdot 0.05 / (dI/dt)$

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From the foregoing explanations follows that, with given parameters of an electronic circuit (operating voltage, transient tolerance, current change rate), by application of the present patent the error-free operating frequency of the electronic circuit when miniaturizing it, by a factor of e. g. 10,000 to 1 by integrating it within a semiconductor chip, can theoretically be increased by a factor of 10,000, compared to the error-free maximal operating frequency of the conventional arranged electronic circuit that has not yet been miniaturized.

Current change compensation circuits (shunt-voltage regulators) that are comprised of the same transistors as the electronic functional units can be miniaturized by the same ratio as the functional units themselves without losing effectiveness. In contrast capacitors lose capacitance with the 3rd degree when being miniaturized and with that they lose their ability of effective current change compensation.

II. On-chip data transmission:

The planned performance increase for microchips via a raise of the operating frequency to about 15 GHz and above, that has been announced by leading chip manufacturers back in 2004, never happened in the past ten years and not up to the present day.
The on-chip data transmission between CPU cores and memory units over a few millimeters via interconnects found a practical limit at about 250 MHz due to the interconnect capacitance and the low wave impedance of about 40 to 60 Ω. As a workaround to get higher data rates, at operating frequencies between 1 to 5 GHz, chains of inverters (repeaters) have been used.
Disadvantages of these inverter chains are a great wastage of chip area with an according high power dissipation and high chip temperature at increasing clock frequencies. The biggest disadvantage of these inverter chains however is their delay time which decreases the data propagation time to around 2,000 km per second and thereby restricts a further increase in clock frequency.
On-chip optical data transmission is meant to lead a way out of this dilemma. Problems of this solution are: High wastage of chip area and the data conversion of electrical impulses into light impulses and back into electrical impulses. With optical on-chip data transmission a data transfer rate of two-thirds that of the speed of light (in the optical fiber) is aimed to be achieved. This would be a data transfer rate that is about 100 times higher than present conventional technologies.
The better, lower priced solution without the expensive conversion of electrical current signals into light and vice versa if offered by the patent application PCT/DE2005/001831 (US 8,466,663) in conjunction with proven semiconductor chip technology.
C-MOS driver circuits (transistors of about 180 nm structural width) combined with current change compensation circuits (as shunt current regulators within µm distance) are, given a shunt current of 20 mA and a supply voltage of 1 V, capable of transmitting data at 100 GHz and above via interconnects (having a width of 1 µm) with a wave impedance of ≥ 50 Ω, without much loss of pulse voltage.
Thereby the same data transfer rate gets achieved as it is possible with optical transmission but with a distinctly lower chip area wastage and lower power consumption.
The design and production of high performance microprocessors with clock frequencies above 100 GHz on basis of proven semiconductor chip technology is made possible by making use of the patent application PCT/DE2005/001831 (US 8,466,663).

Next page gives a more lucid view of the original patent drawing FIG. 1

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The figure below shows the typical configuration of a chip supplied by a point-of-load converter with supporting capacitors C_{PPC} and C_{INT}. The integrated circuit broken down into microscopic level is to be considered as the sum of its individual LOADs within. Usually, they have power feed lines such as I1.1, I1.2, I2.1, I2.2, I3.1 and I3.2 for supply, thus the inductance of all these feeders becoming operative. However, if a switching element -the placeholder of which here is named DSK- capable of compensating current changes is matched to every LOAD, the effective inductance will shrink to feed lines like I3.1 and I3.2 between the LOAD and its switching element DSK. Adapted to the integrated circuit design and scaled to the expected needs of power (examples given for the broad variety of possibilities are a reverse-coupled N-Channel-MOSFET and a Zener-Diode) the element DSK is able to provide current carried by itself (I_{DSK}) to a LOAD or vice versa to take over current abundant through a temporary under-consumption of a LOAD. Current changes therefore only occur on individual feed lines such as I3.1 and I3.2. The current carried by I1.1, I1.2, I2.1 and I2.2 remains nearly constant. For the scale of I3.1 and I3.2 is less than 1/1000 that of I1.1 and I1.2, the proportional operative inductance is reduced to 1/1000 compared to power supplies according to the state of the art. Moreover, transients of the supply voltage U_B will be equally reduced. Noise problems get eliminated.

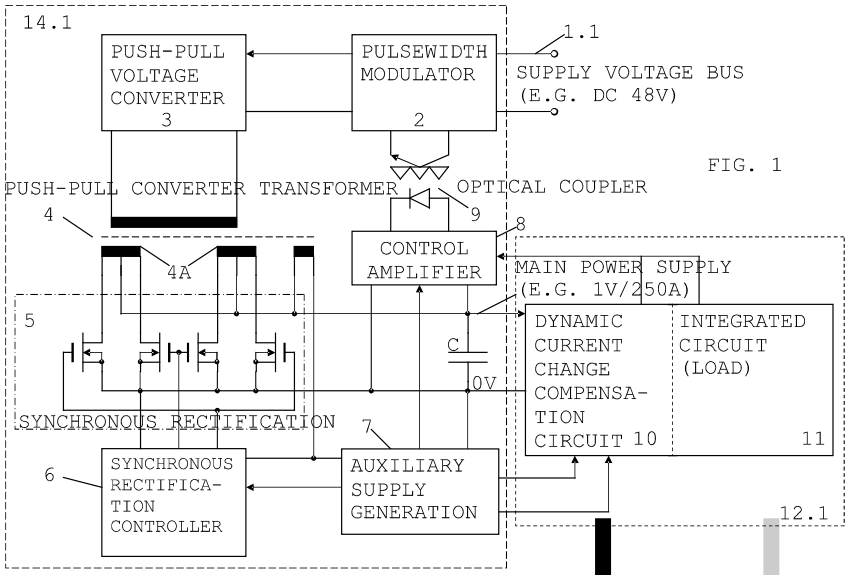

FIG. 1